ABUBAKAR TAFAWA BALEWA UNIVERSITY, BAUCHI

FACULTY OF ENGINEERING AND ENGINEERING TECHNOLOGY

DEPARTMENT OF ELECTRICAL/ ELECTRONICS ENGINEERING

Yelwa Campus, P.M.B. 0248, Bauchi, Nigeria

Vice Chancellor:
Prof. M. A. Abdulazeez, B.Tech(Yola) , M.Sc (Ibadan) ,
Ph.D. (A.T.B.U)

Head of Department:
Prof. Y.S. Haruna, B. Eng.(ATBU), M.Eng.(ATBU),
Ph. D. (A.T.B.U.). MNSE, RE- COREN

Our Ref:_____
Your Ref: NCC/R&D/ATBU/13

Date: 21th March 2023

The Head, Research & Development
Research & Development Department
Nigerian Communications Commission
Plot 423 Auiyi Ironsi Street
Maitama District, Abuja

Dear Sir,

FINAL REPORT ON

(IMPLEMENTATION OF A LOW COST MICROWAVE OSCILLATOR FOR 0.9 TO 8GHZ RANGE)

I hereby humbly submit the final report or the project Implementation of a Low Cost Microwave Oscillator for 0.9 To 8GHz Range attached herewith.

Yours faithfully,

Lead Researcher Prof. E. C. Anene,

Co Researchers: Engr. Mahmood Abdulhameed

Engr. Muhammad Sani Yahaya

A LOW COST MICROWAVE OSCILLATOR FOR 0.9 TO 8GHZ: DESIGN, SIMULATION AND IMPLEMENTATION

In designing a microwave oscillator, an important factor to consider is the appropriate choice of transistor for low phase noise and frequency stability.

At microwave frequencies, Scattering or S - parameter method is the most preferred choice for oscillator design because it is very difficult to measure voltage or current directly at these frequencies.

S - parameters are useful design aids that most manufacturers supply for their high frequency transistors. These are widely used because of their ease to measure and work with than Y-parameters, while S-parameters used normalized incident and reflected travelling waves at each network port. However, with S - parameter, there is no need to present a short circuit to the two-port device. Instead, the network is always terminated in the characteristic impedance of the measuring system.

DESIGN OF OSCILLATOR 1

Figure 1 presents an oscillator circuit designed to oscillate at 8 GHz using ATF-36077 Bipolar Junction Transistor (BJT) with common emitter configuration. The bias points of the transistor were set at [1-2] , I_C = 5 mA, $V_{CE} = 2V$, $h_{fe} = 180$, $V_{BE} = 0.7\,V$, and $V_{CC} = 5\,V$ in order to achieve the condition of stable oscillation i. e. (K <1, $\Gamma_{in}\Gamma_g = 1$, $\Gamma_{out}\Gamma_L = 1$) as obtained by equations (1) – (4).

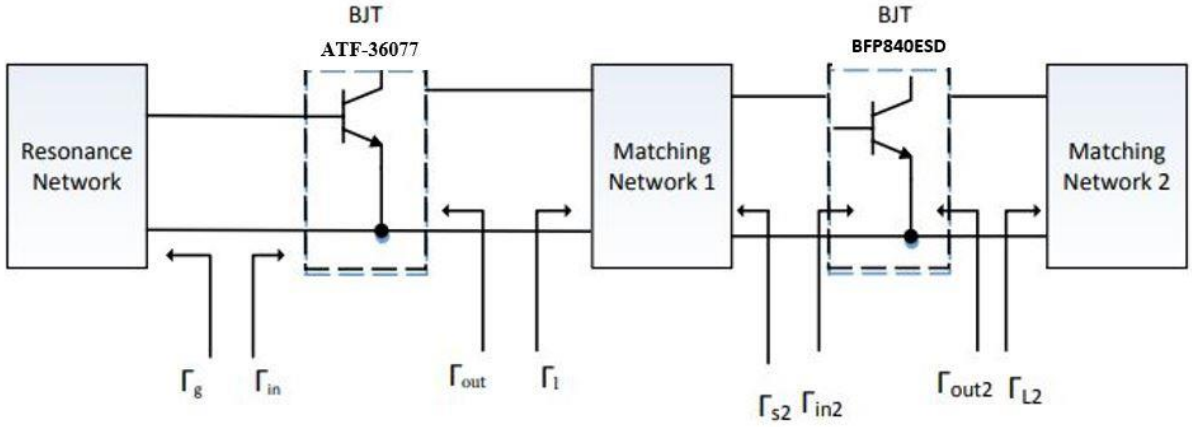

Figure 1: Oscillator with One stage Amplification

$$K = \frac{1+\left|\Delta\right|^2-\left|S_{11}\right|^2-\left|S_{22}\right|^2}{2\left|S_{12}S_{21}\right|} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}$ …….. (3)

$\Gamma_{out} = S_{22} + \frac{S_{11}S_{21}\Gamma_S}{1-S_{11}\Gamma_S}$ …….. (4)

The S-parameters of Avago Technologies's ATF-36077 transistor at 8 GHz with Z_o of 50Ω [1].

is presented as:

$S_{11} = 0.759 \angle -120^0$, $S_{12} = 0.078 \angle 8^0$
$S_{21} = 3.820 \angle 62^0$, $S_{22} = 0.46 \angle -99^0$

From (1) and (2) $K = 0.943$. Since the stability factor K <1, it implies that stable oscillation can be obtained. Also, simulation results show $\Gamma_S = 1 \angle -98.45^0$ and $\Gamma_L = 0.245 \angle$-13.216°.

Amplifier Design

Microwave amplifiers formed one of the major electronics components that combined active elements with passive transmission line circuits to provide functions critical to microwave systems and instruments.

Amplification is one of the most basic and predominant microwave circuit functions in the modern RF and microwave systems.

Microwave transistor amplifiers are low cost, rugged, and reliable and can easily be integrated in hybrid and monolithic integrated circuitry.

The design specifications consist of 8.0 GHz operating frequency, microstrip line with substrate Ɛr = 4.5, thickness of 1.6mm and tan of 0.019. The primary design goal of microwave amplifier is to obtain maximum value of gain.

An important and significant factor in amplifier design is careful and proper selection of transistor. Usually, the biasing point is chosen in such a way that it will keep the transistor in active mode for different forms of circuit technique.

The amplifier was designed using BFP840ESD BJT set at the following bias points:

I_C = 5 mA, $V_{CE} = 2V$, $h_{fe} = 200$, $V_{BE} = 0.7\,V$, and $V_{CC} = 5\,V$.

Its S - parameters were as follows:

$S_{11} = 0.544 \angle -104.263^0$, $S_{12} = 0.051 \angle 8.229^0$
$S_{21} = 3.326 \angle -11.717^0$, $S_{22} = 0.480 \angle 138.430^0$

The first step in the design of an amplifier circuit is determining the stability of the active device i.e conditionally stable or unconditionally stable.

Oscillations are possible in a two-port network when a negative resistance is presented by either the input or the output port. This occurs when $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$, which for a unilateral device ($S_{12} \cong 0$) is when $|S_{11}| > 1$ or $|S_{22}| > 1$. But in practical cases S_{12} is not equal to 0 and thus the unilateral assumption cannot be made.

Unconditional stability of a two-port network at a given frequency is said to occur if the real parts of Z_{IN} and Z_{OUT} are greater than zero for all passive load and source impedances. For bilateral cases (S_{12} not equal to 0) the condition K > 1 is only a necessary condition for unconditional stability where K is the Rollet's factor or stability factor.

Using (1) – (4), $K = 1.786$ at 8 GHz. Since $K > 1$, it means the amplifier is stable at the designed frequency. Also, $\Gamma_{S2} = 0.547\angle$- 115.177^0 and $\Gamma_{L2} = 0.478\ \angle$-$154.09^0$.

Testing for stability in amplifier design is a necessary step because different conditions require appropriate design methods. Before an amplifier is built, it is possible to calculate its potential instabilities in transistors. This calculation serves as a useful approach in finding a suitable transistor for a particular application. Achieving unconditional stability of the circuit is among the goals of the designer. Unconditional stability means that any load present at the output of the device will not oscillate.

Advanced Design System (ADS) by Agilent, Matlab and Proteus software were used to design and simulate the complete oscillator circuit shown in Figure 2.

It can be seen that impedance matching networks were incorporated in Figure 2 in order to compensate for the impedance mismatch in the circuit because Maximum power is delivered when the load is matched to the line and power loss in the feed line is minimized. Impedance matching of sensitive receiver components (such as antenna, low noise amplifier, etc.) improves the signal-to-noise power ratio of the system.

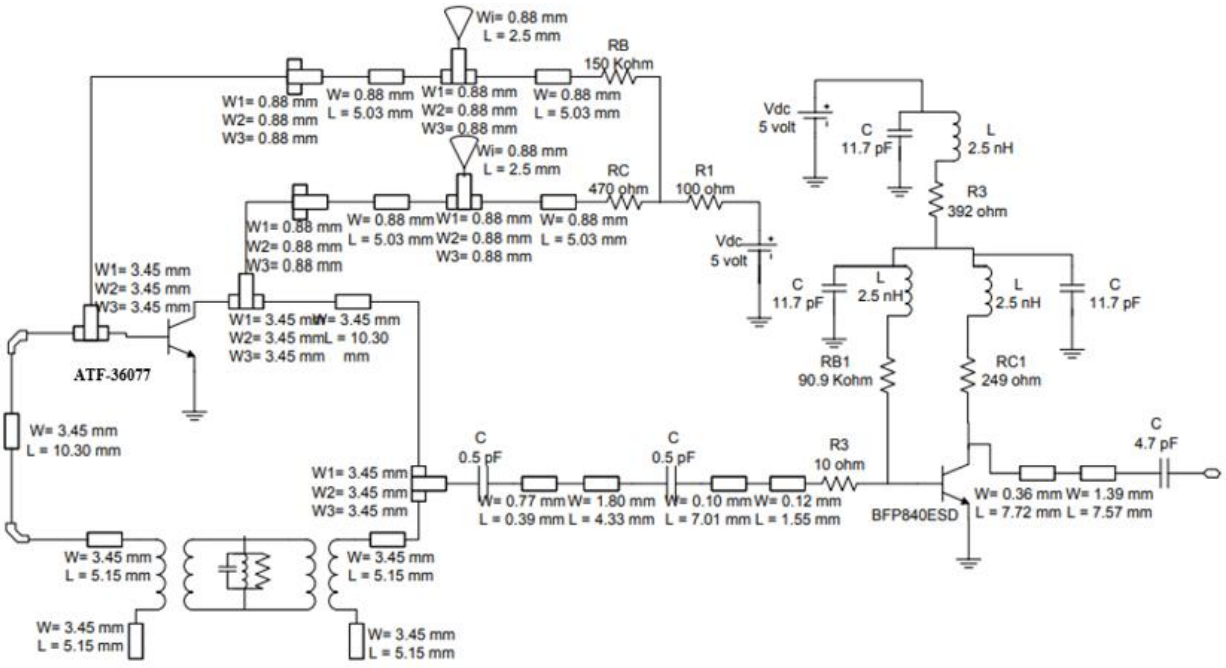

Figure 2: Circuit Diagram of the oscillator 1 in ADS platform

OSCILLATOR 1- SIMULATION RESULTS AND DISCUSSION

The two important parameters that determined the performance of an oscillator are: Output power and phase noise.

Figure 3 show the simulation result of the output power of the oscillator designed at 8 GHz.

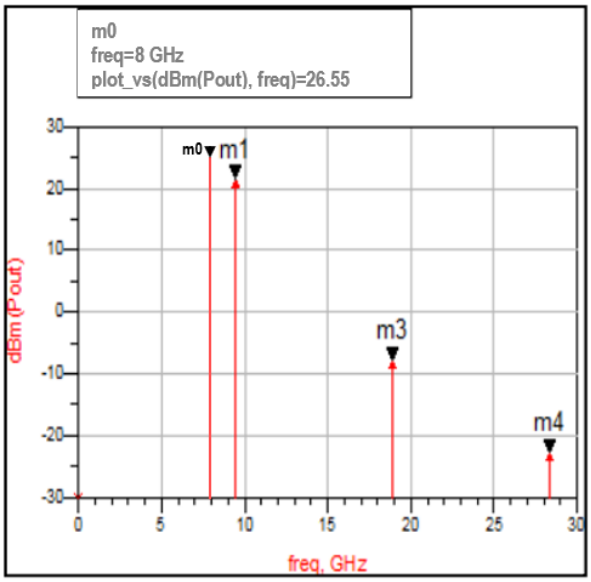

Figure 3: Output Power of the Oscillator

It can be seen that at the designed frequency, the oscillator has achieved an output power of 26.55 dBm.

Figure 4 shows the simulation result of the phase noise of the oscillator. It can be seen that at 100 kHz offset, the simulated phase noise was obtained to be -125 dBm/Hz. This indicates a low phase noise performance because most of the reported oscillators have phase noise between -100 dBc/Hz and -120 dBm/Hz at 100 kHz frequency offset.

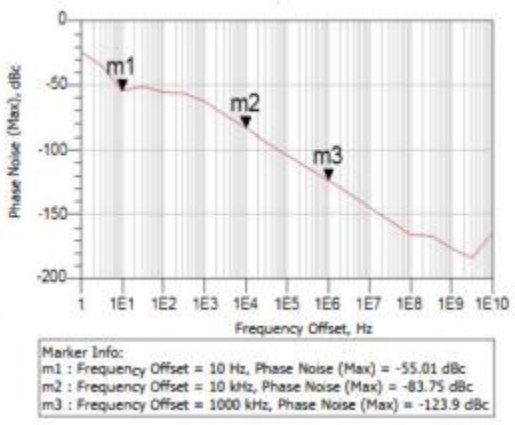

Figure 4: Phase Noise of the Oscillator

Figure 5 is the stability circle of the amplifier at the designed frequency. From the regions on the plot in Figure 5, it showed that the amplifier can operate at 8 GHz without oscillating.

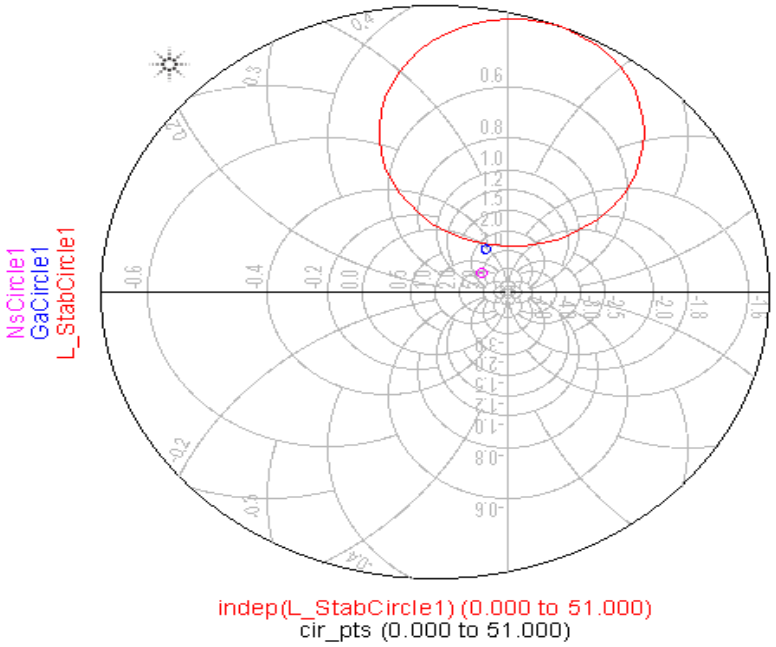

Figure 5: Amplifier Stability Circle

VALIDATION WITH PREVIOUS WORKS

Table 1 gives the comparison between this work and some previously reported literatures.

Author(s)/Freq	[3]/9.75 GHz	[4]	[5]	This work/8 GHz
Output Power (dBm)	9.7	Not mentioned	10	26.55
Phase noise @ 100kHz (dBm/Hz)	-115	-125	-98.7	-125

Based on the comparison in Table 1, the designed oscillator has achieved a high output power and low phase noise.

DESIGN OF OSCILLATOR 2

Skimmed parts of design from [6] detailed below gives a simpler layout that is cheaper to fabricate using the Fr 4 substrate materials for distributed parameters. There are three-transistor configurations that can be utilized to design 2-port oscillators:

1. Common source
2. Common drain
3. Common gate

The common source configuration is selected.

The transistor FPD200P70 (pHEMT) is a depletion mode AlGaAs High Electron Mobility Transistor. It utilizes a (0.25 x 200)μm Schottky barrier gate field effect transistor. The negative impedance circuit in common source configuration utilizing the FDP200P7 transistor is given in figure 6

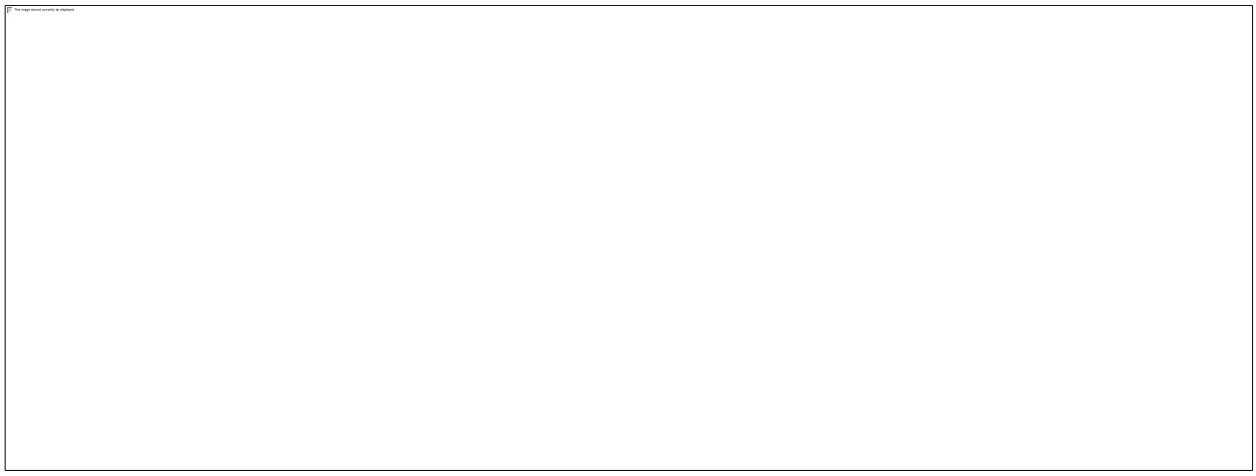

Figure 6: Common Source DC Biasing of FET [6]

Common Source FET DC Biasing:
VDS = 5V
IDS = 30mA
VGG = -15V
I_{DSS} = 60mA
Vt = -0.85V
IDS = 30 mA
VD = 0V
VS = -5V

The design method requires that the transmission lines and the matching terminations be calculated for the frequency of operation.

Method 1 (from IV curve of transistor data sheet)
VGS = -0.45V (from IV curve of transistor data sheet)

$V_G = V_{DS} + V_{GS}$ = -5+ (-0.45) = -5.45
(-5.45) x [R_2/ (R_1+R_2)] = (-15)
R_2 = 1MΩ, R_1 = 2R_2 =1.75 MΩ
Rs = V/I = 10.75/30mA = 378Ω
V= V_{DS} - V_G = -5-(-15.75) = 11.35V

Method 2: (Verifying VGS)
K = I_{DSS}/V_t = 60 mA/ $(-0.85)^2$ = 0.0830
I_{DS} = K [V_{GS} - V_t] = -0.249 > V_t and -1.45 < V_t
$V_G = V_{DS} + V_{GS}$ = -5+ (-0.249) = -5.25
(-5.25) x [R_2/ (R_1+R_2)] = (-15)
R_2 = 1MΩ, R_1 = 2R_2 =1.85 MΩ

$R_S = V/I = 10.75/30mA = 358.3\Omega$
$V = V_{DS} - V_G = -5-(-15.75) = 10.75V$

For biasing network,
f = 18.5 x 109Hz
$Z0 = 50\Omega$
$\omega = 2\pi f = 1.1618 \times 10^{11}$
RF CHOKE:
Z_L is 10 times of $Z_0 = 50\Omega$ and $\omega = 2\pi f$
$Z_L = j\omega L$
$50 \times 10 = 2\pi fL$
L = 4.301 nH
DC BLOCK:
Zcis 1/10 times of Z0
$Z_C = 1/(j\omega C)$
$(5010) = (12\pi fC)$
C = 1.72 Pf

Stability Check:
The common source s-parameters at 18.5 GHz for the transistor are:
S11= 0.688 ∟-4.7°
S12= 0.096 ∟-72.3°
S21= 2.307 ∟-137.3°
S22= 0.593 ∟98.4°
By the above parameters, manually check for the stability using below formulas.
K-parameter:
$= 1-(0.688)2-(0.593)2+(0.34)22|(0.96\angle -72.3° \times 2.307\angle -137.3°)| = 0.65 < 1$
Where,
$= |0.688 \angle -4.7° \times 0.593 \angle 98.4° - 0.096 \angle -72.3° \times 2.307 \angle -137.3°|$
$= 0.34 < 1$
Hence, it is a potentially unstable transistor.

Design of Negative Resistance Oscillator
To design the oscillator, first choose a Γ_T from an unstable region of the output stability circle such that Γ_{in} will be greater than one. This will create a negative resistance at the input port.
$\Gamma_T = 0.93 \angle -115° \; |\Gamma_T| < 1$
$\Gamma_{in} = S_{11} + [(S_{12}S_{21}\Gamma_T)/(1-S_{22}\Gamma_T)] = 1.08\angle 3.26° > 1$ (negative resistance)
$1/\Gamma_{in} = 0.92 \angle 3.26°$
Input port impedance:
$Z_{in} = [(1+\Gamma_{in})/(1-\Gamma_{in})] = -16.2 + 12.4j$ (theoretical value); $50Z_{in} = -810 + 620j$
Plot Γ_{in} on the smith chart to find the input impedance
$Z_{in} = 16 + 12j$ (negating r); $Z_{in} = (-16 + 12j) \times 50 = -800 + 600j$; $R_g = R_{in}/3 = 800/3 = 266.6$
$X_g = -X_{in} = -600j$; $Z_g = ((R_g + X_g)50) = 5.3 - 12j$
Finally,
$Z_T = [(1+\Gamma T)/(1-\Gamma T)] = [(1+0.93\angle -115°)/(1-0.93\angle -115°)] = 0.05 - 0.63j$

Generator Tuning Network Design:
The above Γ_{in} was found to be $1.08 \angle 3.26°$ and therefore, Z_{in} to be
$Z_{in} = [(1+\Gamma_{in})/(1-\Gamma_{in})] = -16.2 + 12.4j$ (theoretical value)
$Z_g = (R_g + X_g)/50 = 5.3 - 12j$

From Fig 7, a resistor with a resistance of 65Ω has been used at point A. The open shunt stub has been used from point A to point B (VSWR and conductance intersection). The distance between these two points are shown below.

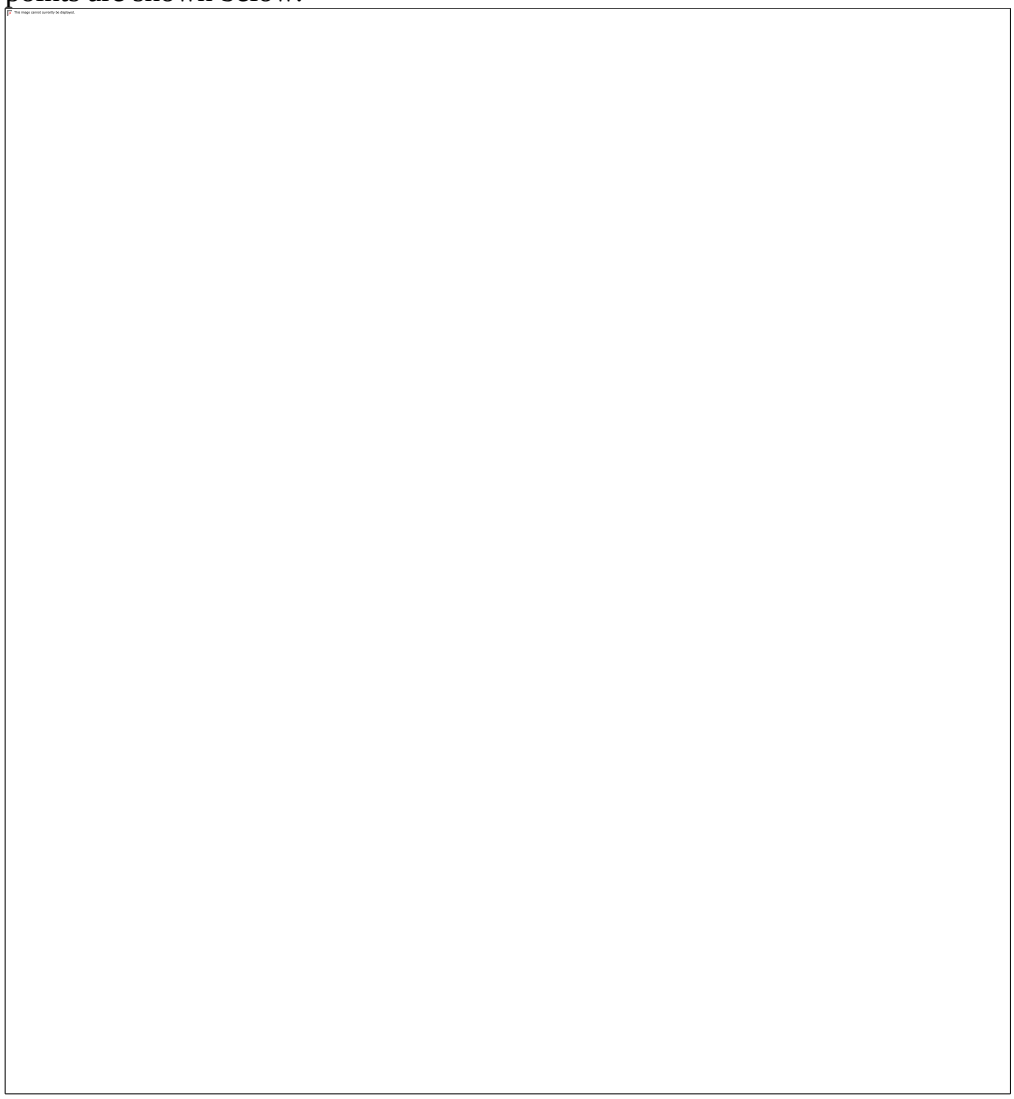

Figure 7: Smith Chart matching for Generator impedance

$\ell AB = (0.43\lambda - 0.25\lambda) = 0.18\lambda$ (open shunt stub)
Next point is to travel, from point B until point G on VSWR circle on the smith chart. The distance between those, two points are shown below.
$\ell_{BG} = (0.500\lambda - 0.434\lambda + 0.261\lambda) = 0.327\lambda$ (transmission line)

Figure 8: Circuit for Generator Tuning network

Terminating Matching Network Design

The above Γ_T was found to be $0.93 \angle -115°$ and therefore Z_T to be $Z_T = [(1+\Gamma_T)/(1-\Gamma_T)] = 0.05 - 0.63j$
From Fig 9 below showing the smith chart, open shunt stub has been used to indicate above from load point 50Ω (point O) to point A (VSWR and conductance intersection). The Distance between those two points is shown below.

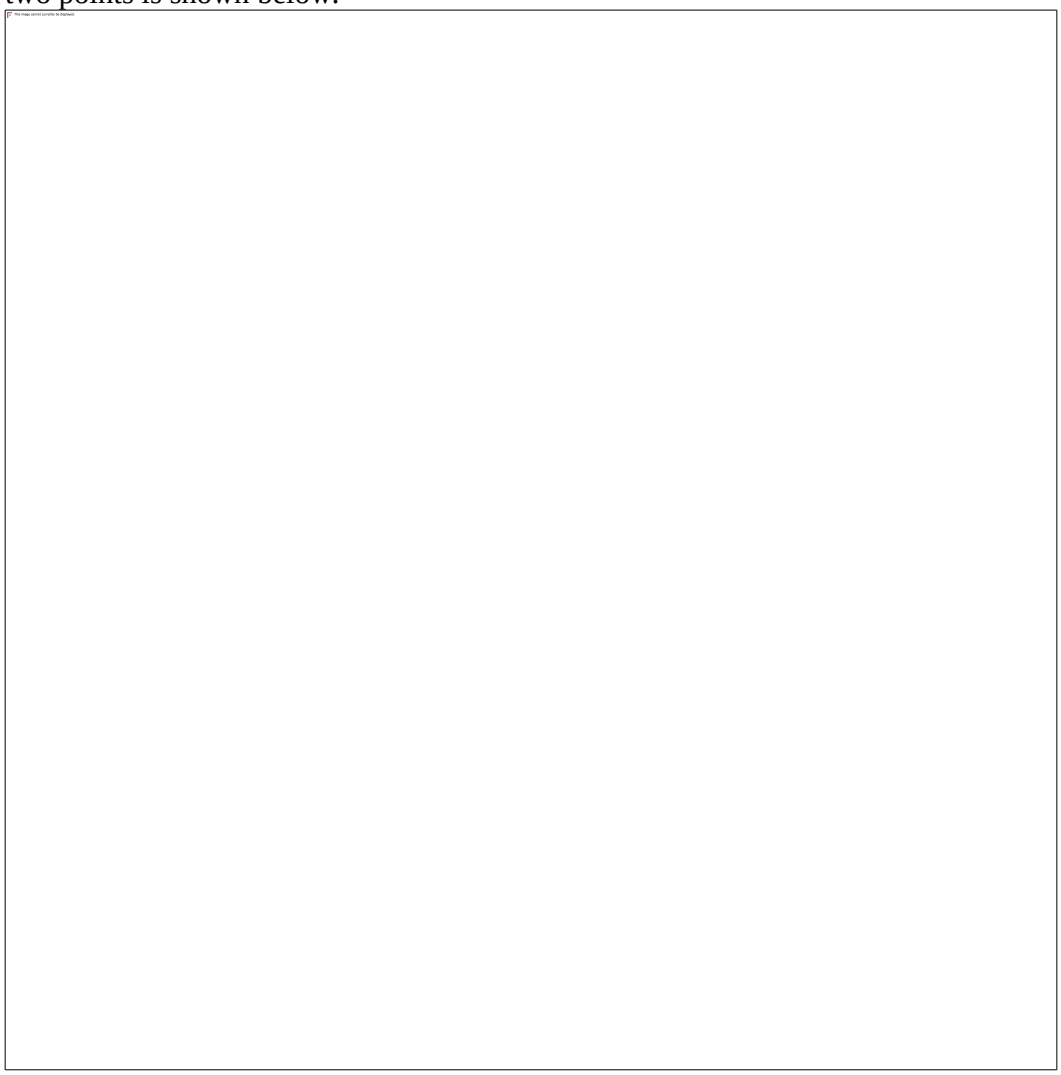

Figure 9: Smith Chart for Matching Termination Network

$\ell_{OA} = (0.47\lambda - 0.25\lambda) = 0.22\lambda$ (open shunt stub)

Next point is to travel, from point A to point B on VSWR circle on the smith chart. The distance between those two points is as shown below.

$\ell_{AB} = (0.50\lambda - 0.47\lambda + 0.411\lambda) = 0.441\lambda$ (transmission line)

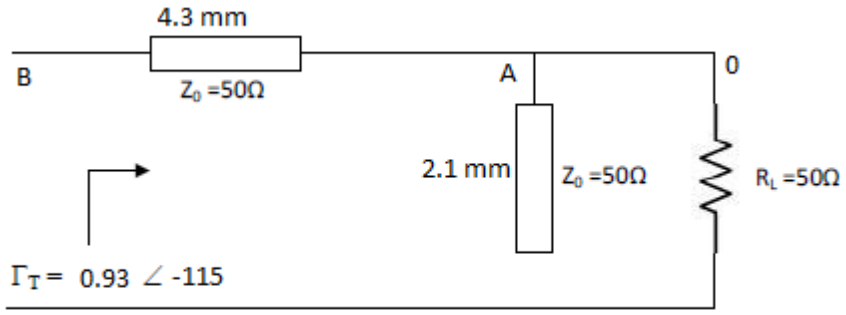

Figure10: Circuit for terminating network

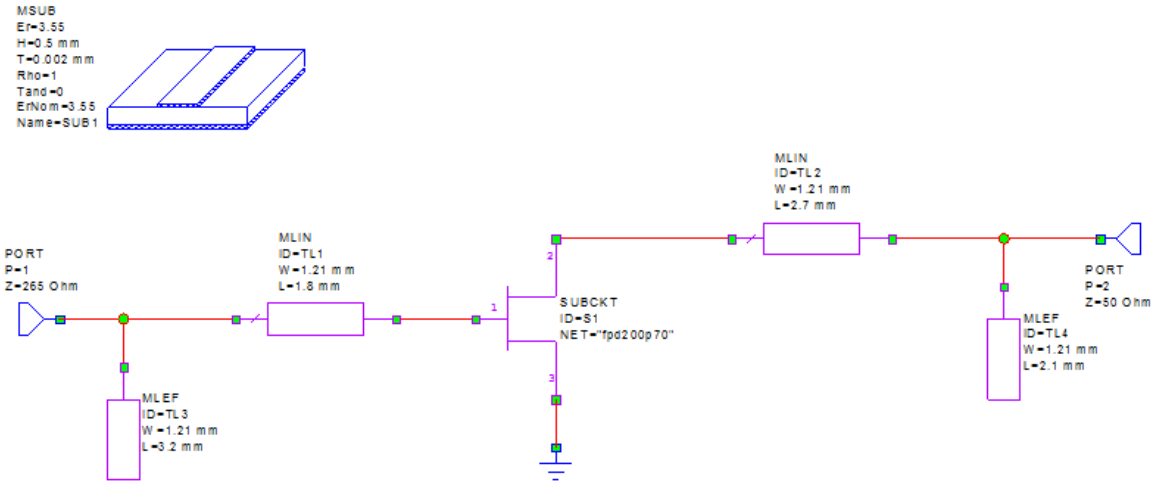

Figure 11: Transmission line circuit for Generator tuning and Terminating Network

Microstrip calculation for transmission line

The transmission line consists of a strip of the conductor with width (w) and thickness (t), which is placed above the dielectric substrate (ε_r) as shown in below figure. In this project, a dielectric constant ($\varepsilon_r = 3.55$) and a dielectric thickness (h = 0.5 mm) is selected based on the Rogers data sheet

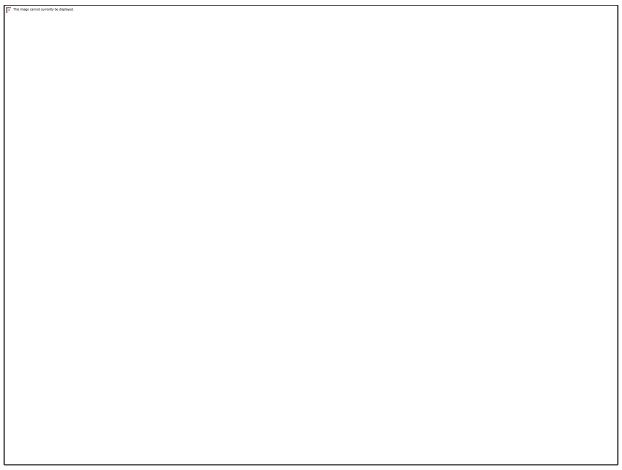

Figure 12: Basic Diagram for Transmission Line

Transmission line of 50Ω is designed based on 18.5 GHz frequency by selecting the ε_r and h from the datasheet available from the Rogers datasheet. By these two specification the remaining width, wavelength, and ε_{eff} are calculated.
f = 18.5 GHz, Z_0 = 50Ω, C = 3 x 10^8 m/s, $\lambda o = c/f$ = 16.2 mm 26
W = 2.27 x 0.5 = 1.13 mm

Length of the terminating network
Open shunt stub:
$\ell = 0.22\lambda$ = 0.22 x 9.7 = 2.13 mm
Transmission line:
$\ell = 0.441\lambda$ = 0.441 x 9.7 = 4.27 mm

Length of the generator-tuning network
Open shunt stub:
$\ell = 0.18\lambda$ = 0.18 x 9.7 = 1.76 mm
Transmission line:
$\ell = 0.327\lambda$ = 0.327 x 9.7 = 3.17 mm

Microstrip calculation for Characteristic impedance:
W = 2.27 x 0.5 = 1.13 mm
ℓ = W/3 = 0.38 mm

Quarter wave transformer:
$\lambda_g = \lambda \sqrt{\varepsilon_{eff}}$ = 16.2 / √2.48 = 10.28 mm
$\ell = \lambda_g/4$ = 10.24/4 = 2.57 mm
To find width consider Z_0 = 120Ω

W = 0.40 x 0.5 = 0.2 mm

By exact and graphical method, it is confirmed that at w/h (0.4), characteristic impedance (Z_0) is found to be 120Ω.
W1 = W2 = 1.13 mm (from layout), Cs = 1.72 pF, h = 0.5 mm
$Q1 = 0.04598(0.03+(W1/h)^{Q5})(0.272+0.07\varepsilon_r)=0.066$
$Q5 = 1.23/(1+0.12((w2/w1)-1)^{0.9}) = 1.23$

C_s [pF] = (500 h) (exp (-1.86 s/h) Q1 (1+4.19(1-exp (-0.785√hw2/w1w1))))
S = (log (Cs/500 h Q1 (1+4.19(1-exp (-0.785(√(h/w1))w2/w1))))/h) x (-1.86) = 0.38mm

Cut-off frequency: (f_0)
f_0 (GHz) = 0.3√(Z_0 / h√(εr−1)) (h should be in cm)
Where, Z_0 = characteristic impedance, h = height, ε_r = 3.55, h = 0.5 mm
f_0 (GHz) = 0.3√(50 / 0.05√(3.55−1)) = 7.5 GHz

Figure 13 shows the designed circuit layout

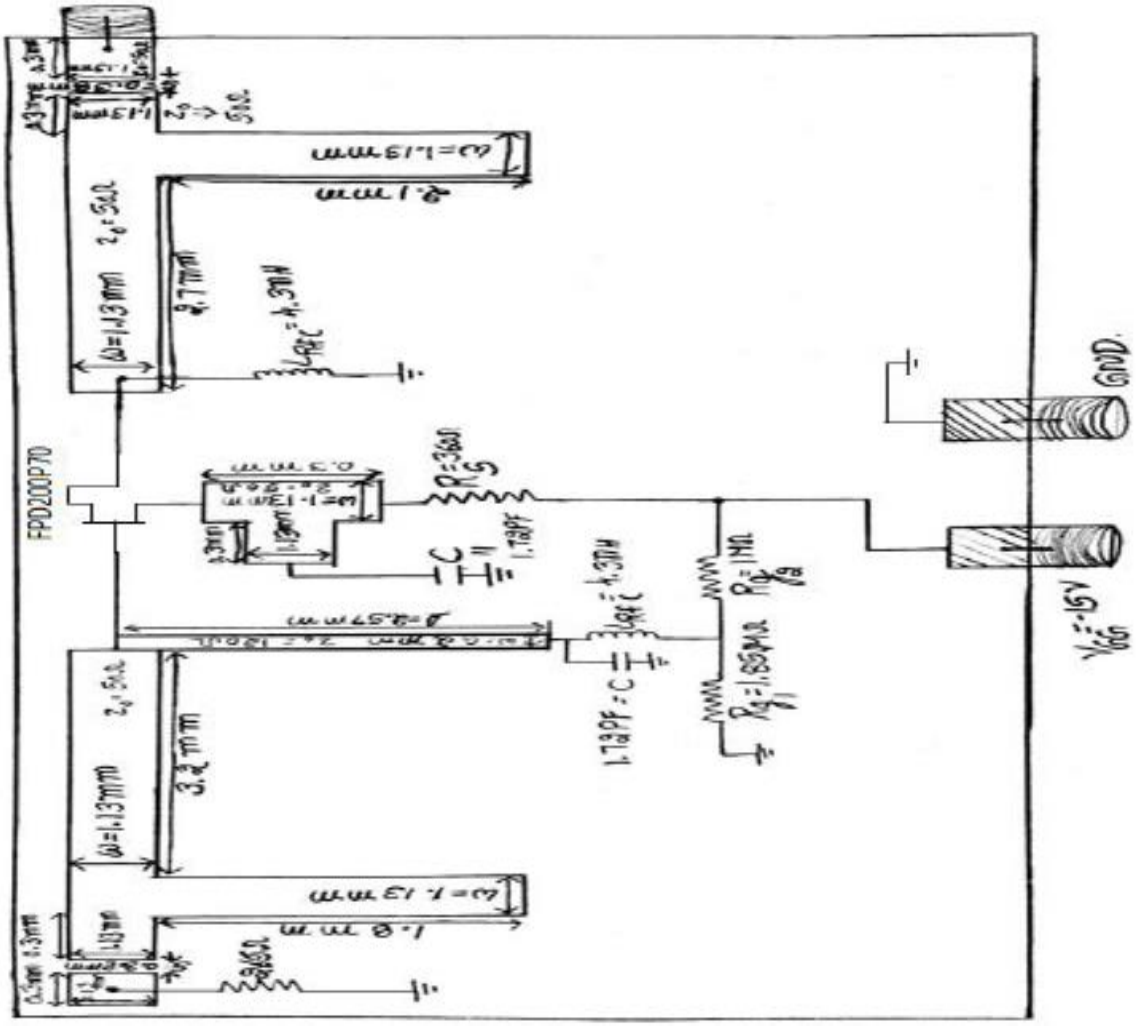

Figure 13: Layout for the negative resistance oscillator design

FABRICATION OF PROTOTYPE

This last part of the work has to do with fabricating the prototype of the 8GHz oscillator. From design calculations a cutoff frequency of 7.5GHz is expected. Being a high frequency system, fabrication must be done very carefully in an automated or semi-automated environment, to drastically minimize presence of parasitic components that may negatively affect the performance. Such parasitic components come from unwanted inductance and capacitance and create

mismatches in the circuit. The design circuit of oscillator 1 was not fabricated due to costs as presented in report 3.

The components of the oscillator 2 circuit in fig. 13 are adjusted to values closest to design values which are obtainable in the market. Presented in figure 14 below are the adjusted component values of the circuit.

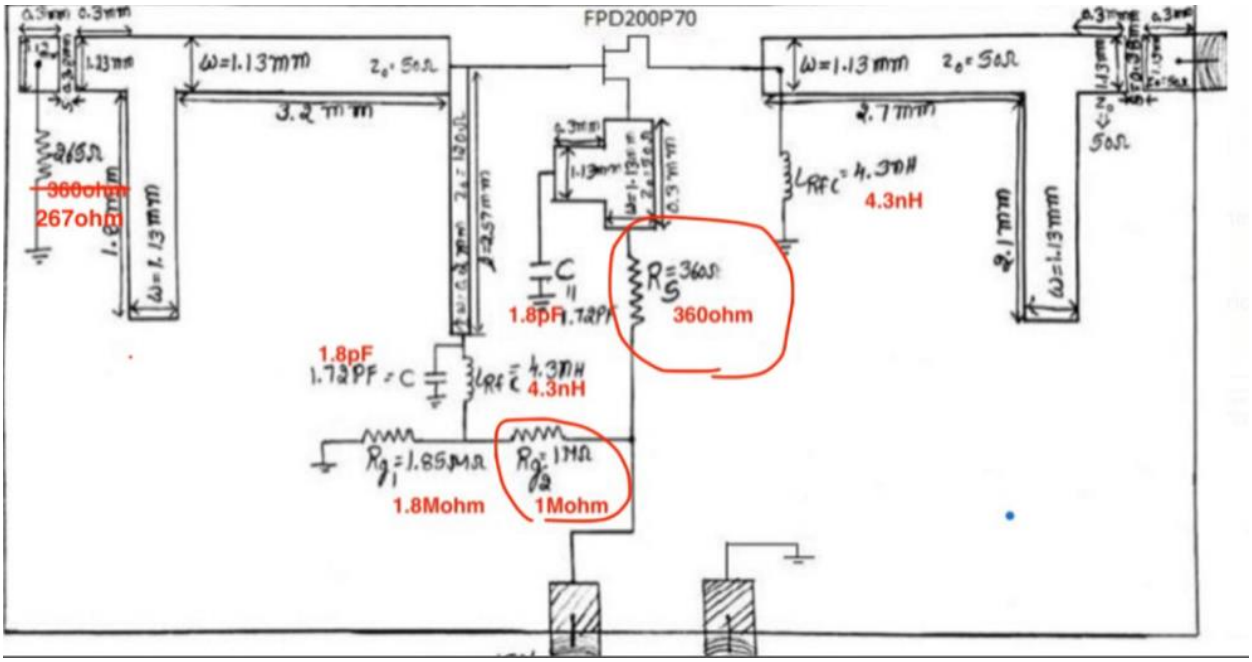

Figure 14: Adjusted component values of the designed circuit.

The fabrication requires etching all transmission lines to the designed dimensions and the layout is first designed in Proteus to cut out solid copper lines from the Fr4 copper clad board. All places where components are to be soldered are opened with the equivalent dimensions that will support easy placement and avoid parasitic inducements. Figs. 15, 16, 17 shows the Proteus bit map profile without and with the components placed in surface mount positions in the required spaces. The spaces for component placement are adjusted in Fig 16. The profile in Fig 17 and the associated Gerber files will be used to set the machines for auto etching, placement and soldering of the circuit to precision dimensions calculated in the design.

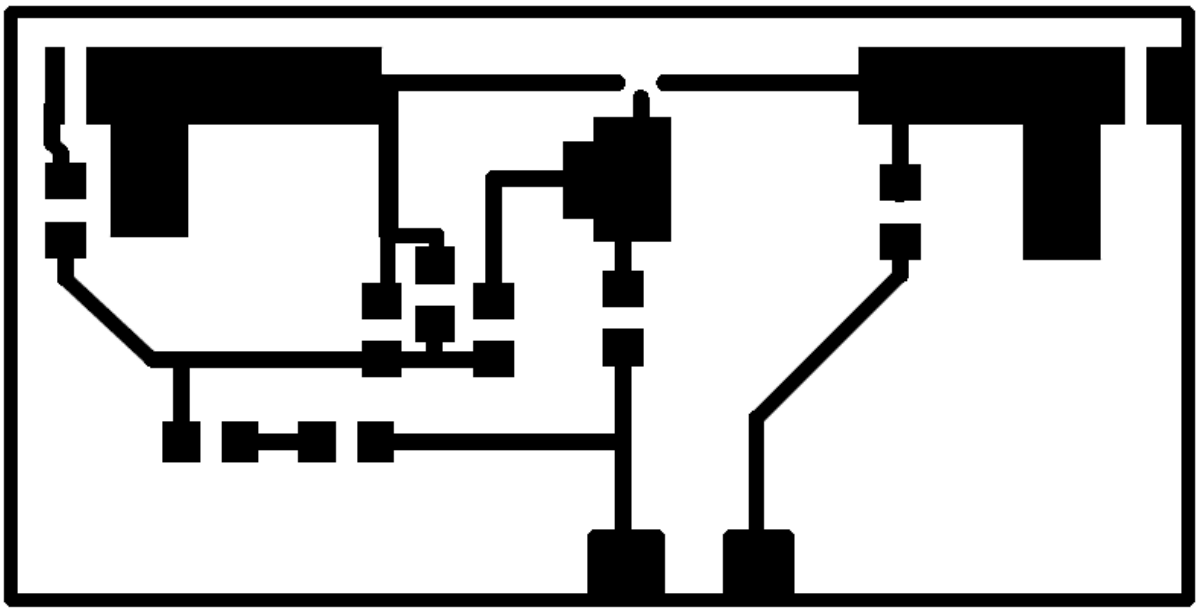

Figure 15: Circuit layout for Etching PDF

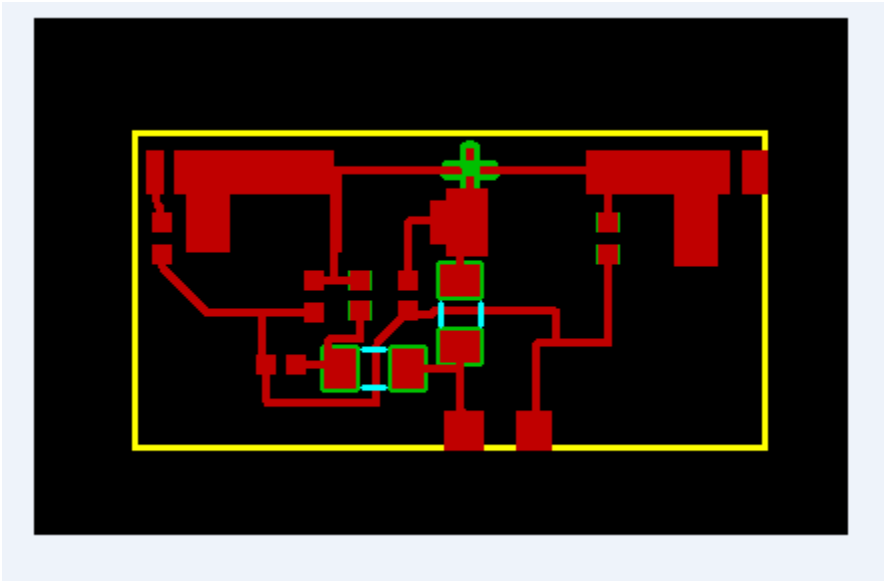

Figure 16: Adjusted Bit Map Layout for Etching

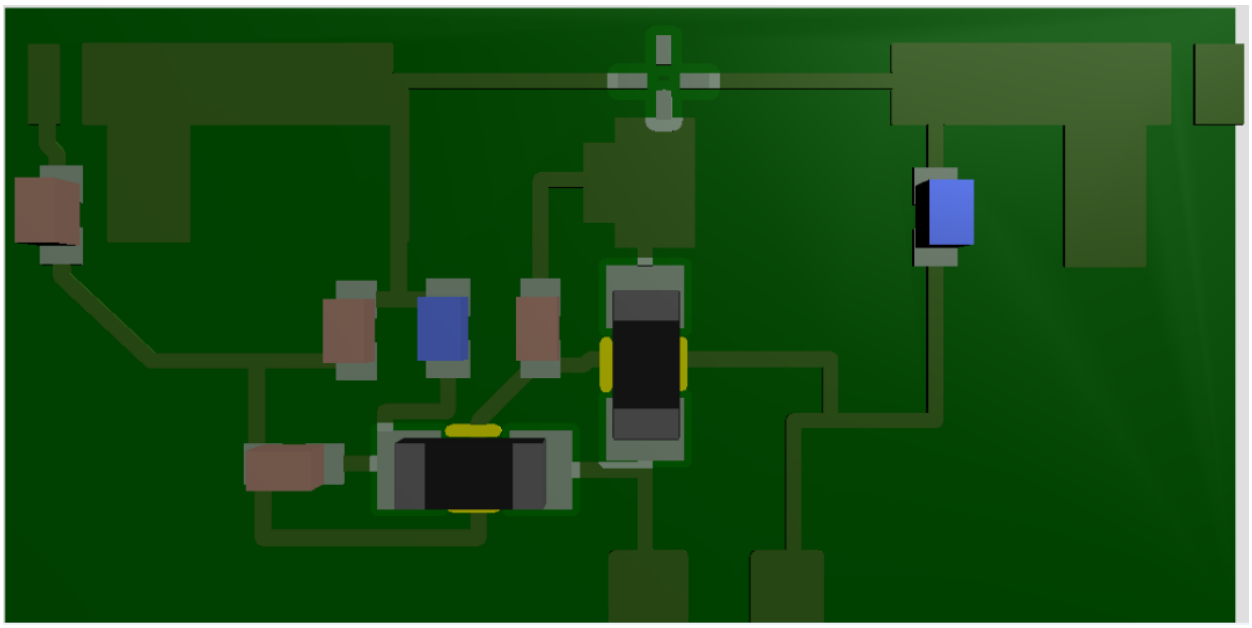

Figure 17: Proteus Bit Map Layout for Etching

Figure 18 shows the Proteus 3D layout of fig 17 in inverted format to show how it will appear in real life.

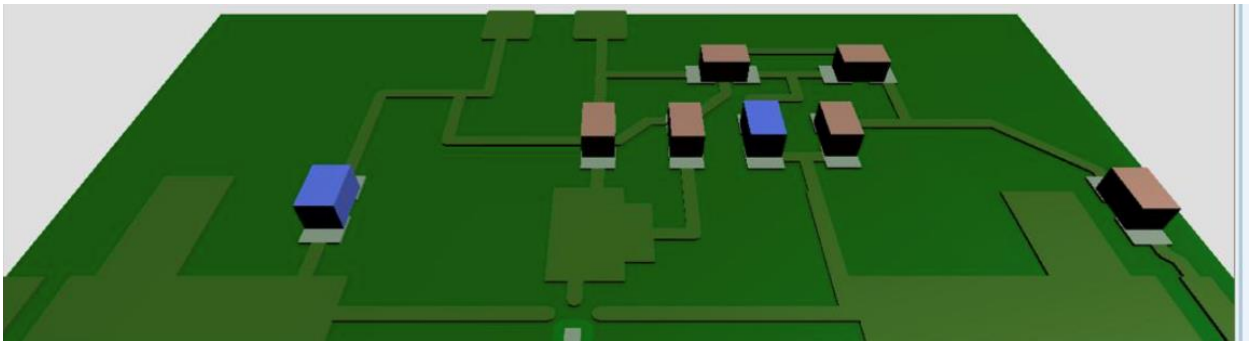

Figure 18: Inverted Proteus 3D layout of Oscillator Circuit

Manual Fabrication for Oscillator 2 design.

Manual fabrication was first done in the laboratory and workshop using components bought at the local market and scavenged from scrap. The Proteus bit map design circuit was used to etch the low value substrate sourced in the local market. It was also extremely difficult to obtain the exact components from the market as the high frequency materials are not on sale and components sourced from scraps. Plates 1 and 2 are the manually fabricated circuits on oscillator 2 design. The circuits did not oscillate because of component mismatch, and lack of ground plane.

Manual Fabrication gives room for induced parasitic components through component spacing, flying leads, component layout, cold solder, and such like. It is also very difficult to make a manually fabricated circuit to be compact thus affecting its size.

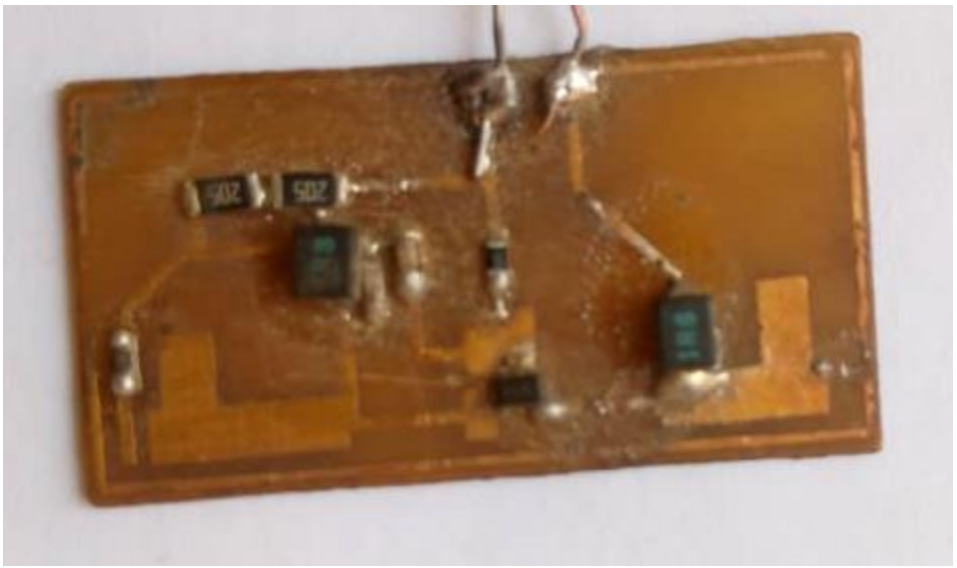

Plate 1: Manual Fabricated circuit 1

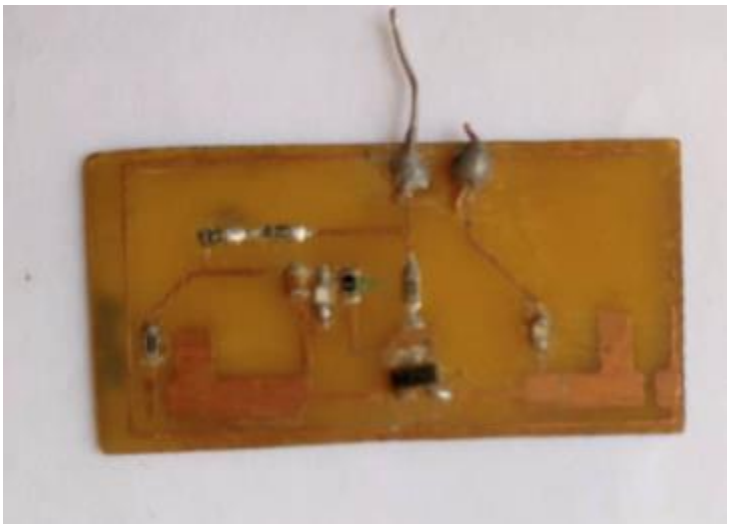

Plate 2: Manual Fabricated circuit 2

Testing the manually fabricated oscillator in the Laboratory yielded no output. This is because of the uncertainty of the exact values of the components used which were sourced from junks and also the lack of fabrication of the transmission lines and matching circuits according to the stringent specifications of length and width.

Plate 3 is the auto fabricated circuit on Fr4 PCB from oscillator design 2. This was done from the information extracted the Gerber files sent to PureTech Computers and PCB services in Malaysia. Plate 4 shows the fabricated oscillator on 0.8mm and 1.6mm fr4 substrates.

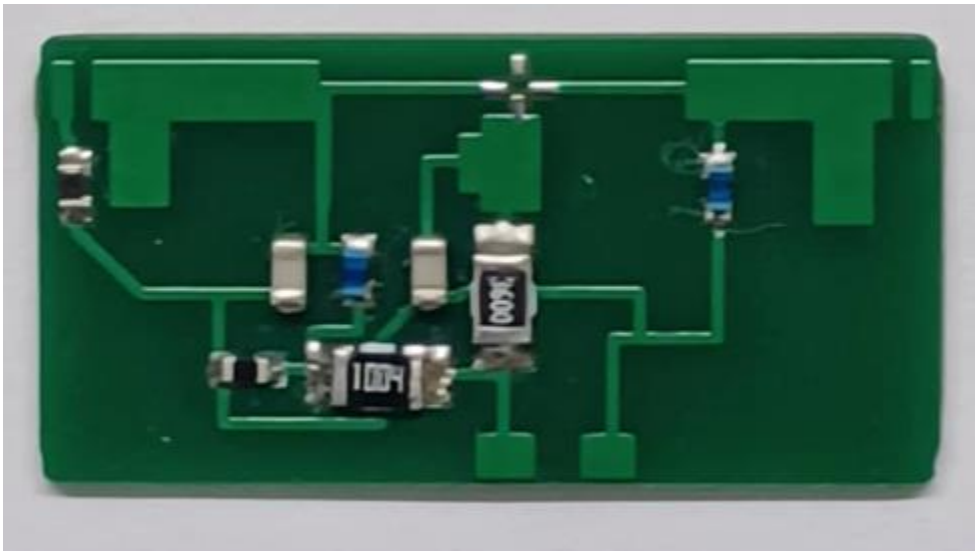

Plate 3: Fabricated oscillator layout on Fr4 substrate

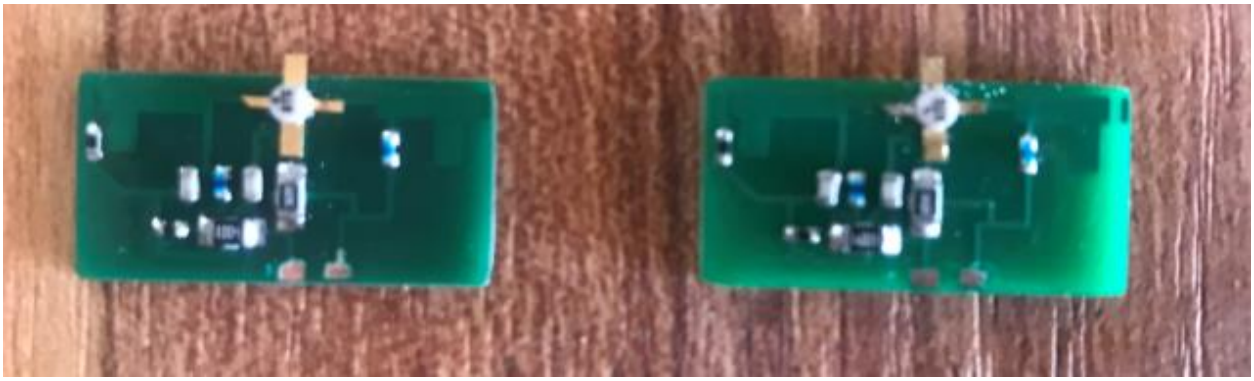

Plate 4: Fabricated oscillators on .8mm and 1.6mm Fr4 substrates

Plate 5 shows the laboratory test rig for testing the oscillators. Use is made of a laboratory standard power supply and 20GHz frequency counter. Plate 6 shows the measured frequency of the fabricated oscillator at 5GHz. The circuits were fabricated at an approximate unit cost of N40,000 each. This cost will be better if the fabrication machines are sourced from Nigeria.

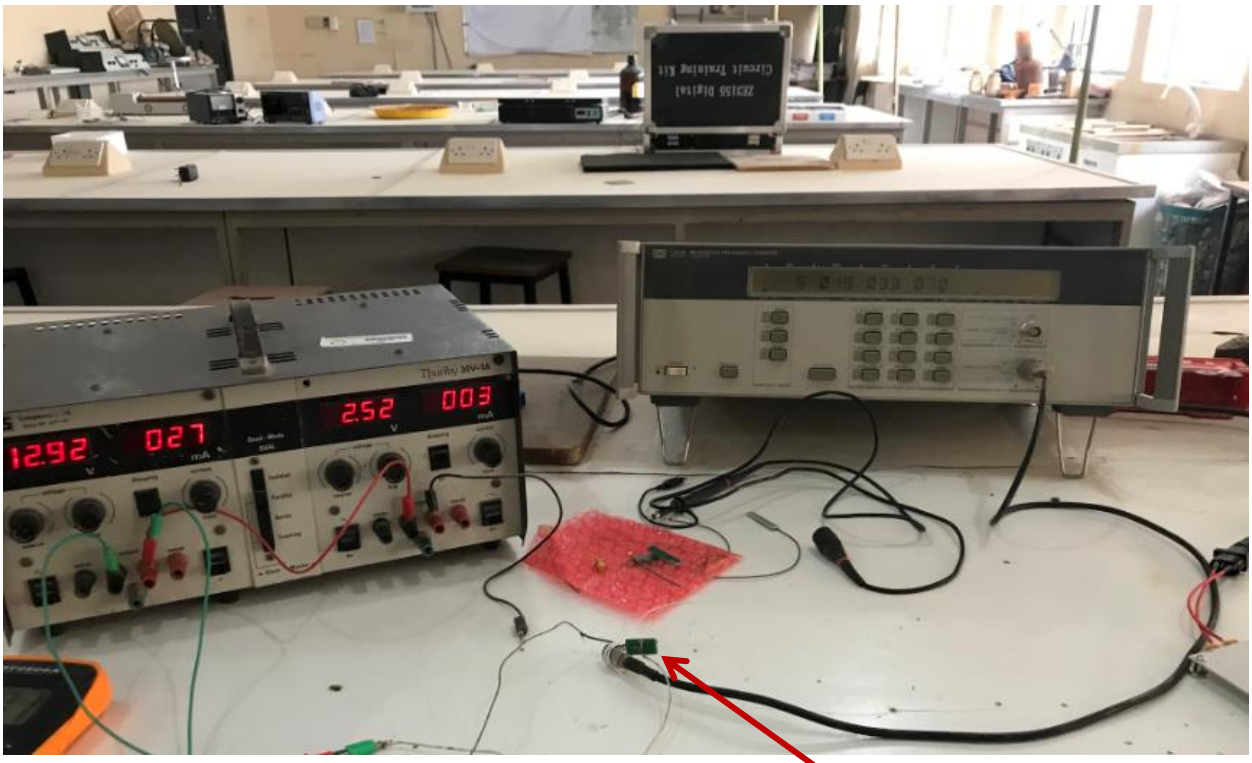

Plate 5: Rig for Testing the Oscillator.

Plate 6: Frequency generated by the Oscillator

Other close-up views of parts of the test rig are shown in Appendix on Plates A1and A2.

DISCUSSION

The cut off frequency from the s-parameter design was at 7.5GHz. The frequency obtained during testing was 5GHz. The shortfall was as a result of limitations of precision in fabrication, use of approximated components and lack of use of proper matched terminations. Some of these limitations can be overcome by precision handling and mismatch corrections.

CONCLUSION

In this report, the design and simulation of microwave oscillator 1 at 8 GHz was presented. The oscillator was designed using ATF – 36077 BJT by Avago Technologies. The Simulated oscillator achieved an output power of 26.55 dBm and a comparatively low phase noise of -125 dBm/Hz. The stability circle of the amplifier was plotted, which showed that the amplifier is stable at 8 GHz.

Studies carried out on the design and implementation of a low cost 8GHz oscillator exposed our co-researchers on the use of specialized high frequency software suite (CST) for the design of oscillators and amplifiers. Simulations carried out show that the resulting amplifier achieved the design objective and was stable in the frequency domain of operation.

Also the design of microwave oscillator 2 at 7.5GHz was presented. Manual fabrication was done but achieved no results. The design was sent to Malaysia and auto fabricated on 0.8mm and 1.6mm Fr4 PCB substrates. Tests showed that the fabricated circuit oscillated at 5GHz instead of the designed 7.5 GHz due to mismatches in termination and over approximation of value of components used.

Attached in the appendix is the Laboratory we setup using the NCC grant at the Faculty of Engineering Block A, Yelwa Campus.

Prof. E. C. Anene, Lead Researcher
Engr. Mahmood Abdulhameed, Co Researcher
Engr. Muhammad Sani Yahaya, Co Researcher

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APPENDIX

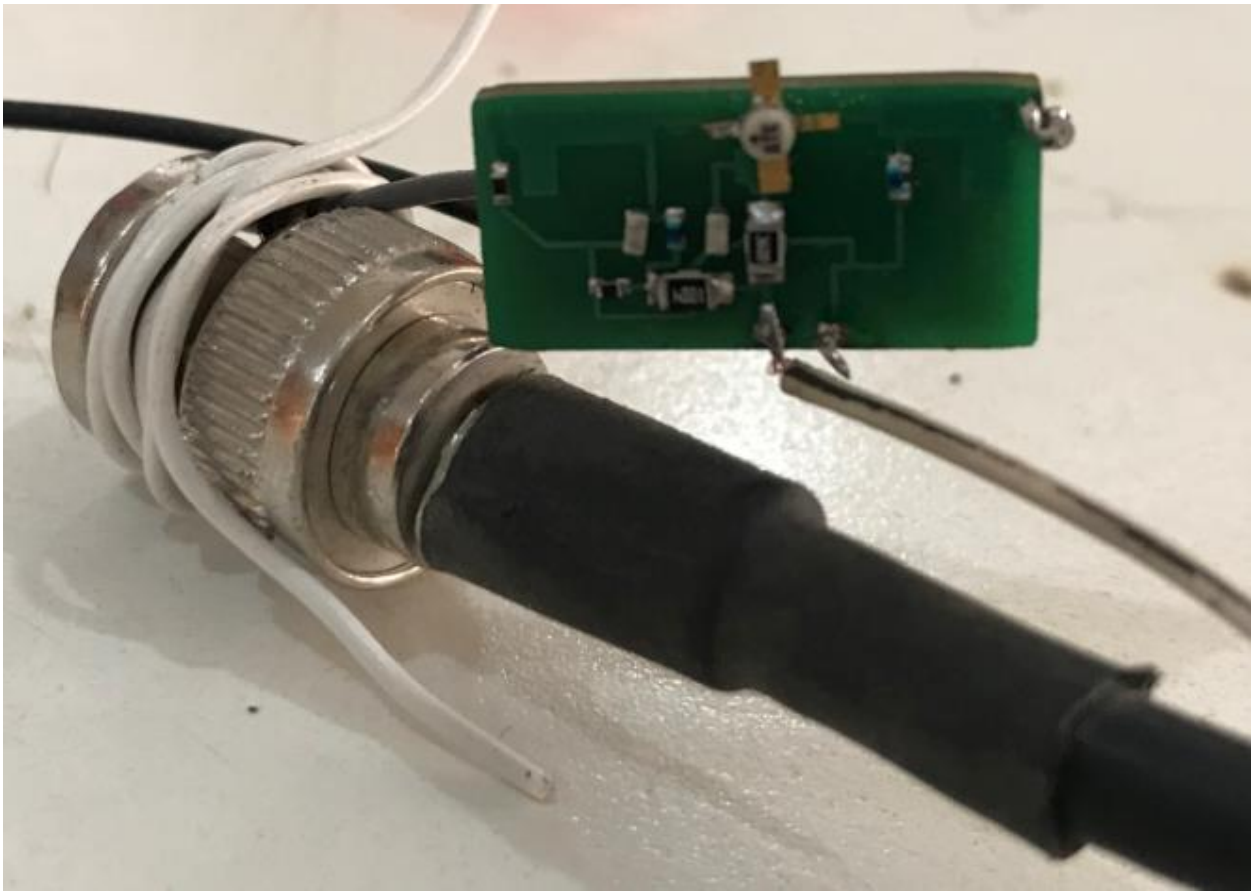

Plate A1, Oscillator circuit connection on Test Rig

Plate A2, Close up view of the Power Supply used and Multimeter.

LABORATORY SPACE

A substantial effort was made to use the opportunity of the project and similar projects to set up a research laboratory in the Faculty. Having been allocated space by the Dean of Faculty of Engineering to this effect, basic computing and simulation software has been procured and installed on the computers purchased for the laboratory using the grant.

The attached photographs show the laboratory space graciously given us by the Dean to set up a Communications and Control Laboratory for research in Block A of the Faculty Building. Through funds from NCC and another project, we have put basic equipment and computer.

Plate A3: Empty Laboratory space before allocation

Plate A4: Laboratory space with some equipment.

Plate A5: Laboratory from a different angle